Claims

1. A memory module, comprising:

a memory configured to store data;

a supplemental information device configured to store supplemental information;

an interface connection connected to the memory and the supplemental information device and configured to operate in a first mode and a second mode, wherein the interface connection:

transfers information to or from the memory in the first mode; and

transfers information to or from the supplemental information device in the second mode.

2. A memory module according to claim 1, wherein the supplemental information comprises configuration information relating to the memory module.

3. A memory module according to claim 2, wherein the configuration information comprises SPD information.

4. A memory module according to claim 1, wherein the interface connection transfers information to or from the supplemental information device in the second mode using SMBus protocols.

5. A memory module according to claim 1, wherein the memory module comprises a chip select connection, and the memory module is selected for information transfers to or from the supplemental information device in the second mode by signaling the memory module via only the chip select connection.

6. A memory module configured to operate in a serial presence-detect (SPD) mode and a normal mode, comprising:

a random access memory (RAM) configured to store information at a location characterized by an address datum;

an SPD device configured to store SPD information; and

an address/SMBus connection connected to the RAM and the SPD device and configured to transfer a datum, wherein:

the datum is transferred to or from the RAM when the memory module is operating in normal mode for processing as the address datum; and

the datum is transferred as a serial system management bus (SMBus) signal to or from the SPD device when the memory module is operating in SPD mode.

7. A memory module according to claim 6, further comprising a second address/SMBus connection connected to the RAM and the SPD device, wherein:

the first connection transfers a serial clock signal for presence-detect signal; and

the second connection transfers a serial presence-detect data signal.

8. A memory module according to claim 6, wherein the memory module comprises a chip select connection, and the memory module is selected for information transfers to or from the SPD device in the SPD mode by signaling the memory module via only the chip select connection.

9. An electronic system having at least two memory modules, wherein each memory module comprises a first connection configured to perform:

a normal function in a normal mode; and

a configuration function in a configuration mode.

10. An electronic system according to claim 9, wherein the configuration function is comprises transferring SPD information.

11. An electronic system according to claim 9, wherein the configuration function comprises transferring SPD information according to SMBus protocols.

12. An electronic system according to claim 9, wherein each memory modules comprises a chip select connection, wherein each memory module is addressed by signaling via only the chip select connection.

13. A memory system, comprising:

a memory controller; and

a memory responsive to the memory controller and comprising a first connection, wherein:

the memory communicates with the memory controller via the first connection to transfer serial presence detect (SPD) information when the memory is in an SPD mode; and

the memory communicates with the memory controller via the first connection to transfer non-SPD information when the memory is in a normal mode.

14. A memory module comprising a multi-function connection, wherein at least one of the functions associated with the multi-function connection is an SMBus interface function.

15. A memory module according to claim 14, wherein:

the memory module operates in multiple modes;

the SMBus interface function is performed by the multi-function connection when the memory module is in an SPD mode.

16. A memory module according to claim 15, wherein the SMBus interface function comprises transferring at least one of a serial clock signal for presence-detect signal and a serial presence-detect data signal.

17. A memory module configured to operate in a normal mode and an SPD mode, wherein:

the memory module comprises a plurality of interface connections;

the interface connections are configured to:

perform a set of memory access functions when the memory module is operating in the normal mode; and

perform a set of SMBus interface functions when the memory module is operating in the SPD mode.

18. A memory module configured to operate in a normal mode and an SPD mode, comprising a first connection and a second connection, wherein:

the first and second connections facilitate communication of non-SPD information when the memory module operates in the normal mode; and

the first connection facilitates communication of serial clock for presence-detect signals and the second connection facilitates communication of serial presence-detect data signals when the memory module operates in the SPD mode.

19. A method for retrieving configuration information for a memory system from the memory system, comprising:

requesting configuration information from the memory system via a first connection of the memory system while the memory system is in a first mode;

receiving the configuration information from the memory system via the first connection;

switching the memory system from the first mode to a second mode; and

accessing a random access memory location in the memory system via the first connection.

20. A method according to claim 19, wherein requesting configuration information comprises accessing a configuration register associated with the memory system.

21. A method according to claim 19, wherein requesting configuration information comprises providing a signal in conjunction with SMBus protocols via the first connection.

22. A method according to claim 19, wherein the configuration information is SPD information.

23. A method according to claim 19, wherein requesting configuration information comprises selecting the memory system via only a chip select connection of the memory system.

24. A method for powering up an electronic system, comprising:

providing power to a memory module having an SPD device and a memory;

placing the memory module of the electronic system in an SPD mode;

requesting an SPD information from the SPD device via a first connection on the memory module;

asserting the SPD information via the first connection on the memory module;

switching the memory module from the SPD mode to a normal mode; and

accessing a memory location in the memory via the first connection.